REMARKS

Claims 1-11 are pending.

Claims 1-11 are rejected.

Clams 1, 4, 7, and 10 are amended to more clearly define the limitations of the present invention.

I. EXAMINER INTERVIEW

The Applicant had an Examiner interview on January 26, 2005. The Applicant explained that some of the claim language caused the Examiner to cite art that the present invention is an improvement upon. In Claim 10, "a logic state" should have been "logic states." In Claims 1, 4, 7, and 10, mixed uses of "first and second logic states with logic one and logic zero" have been corrected to make the language clearer. Likewise, the Applicant discussed with the Examiner that the "keeper" of the present invention only enhanced a particular logic state of the dynamic node when the output was the same particular logic state before transitioning to the opposite logic state. The Applicant also stated that the Examiner cited a logic inverter as the static latch of the present invention. The Applicant pointed out that the cited inverter and the "keeper" device constituted a half-latch as they only latch one of the logic states.

II. REJECTION UNDER 35 U.S.C. § 102

The Examiner rejected Claims 10-11 under *35 U.S.C. § 102(b)*, as being anticipated by U.S. Patent No. 6,404,236 B1 to *Bernstein et al.* (hereafter "*Bernstein*").

The Examiner states that Claim 10 is anticipated by Bernstein and cites FIG. 2 of Bernstein which is a prior art Domino logic circuit. The Applicant has amended Claim 10 to correct the language that caused some confusion.

The Examiner stated that the dynamic logic circuit of Bernstein has an output (output of 23) and a complementary output (OUTPUT), the dynamic node (23), the precharge circuitry (24) coupled to the dynamic node for precharging the dynamic node to a logic one during a precharge of a clock signal (CLOCK INPUT), and a logic tree (21) coupled to the node for evaluating the dynamic node to a logic one or a logic zero in response to combinations of logic states of the plurality of logic inputs coupled to the logic tree during an evaluation cycle of the clock signal. However, the Examiner further states that the static logic circuitry, of element d) above, is element 26, a logic inverter. The simple logic inverter 26 of Bernstein does not latch logic states of the dynamic node and hold these states during the precharge cycle of the clock signal as claimed. The output of Bernstein inverter 26 follows its input which is the dynamic node 28. Furthermore, the static logic circuitry of the present invention generates both the output and the complementary output. The logic inverter of Bernstein only generates one output. The Examiner states that the static logic circuitry of Bernstein generates the output (via feedback signal) which is generated by keeper device 23. Keeper device 23 only generates a complement to OUTPUT when it is a logic zero; when OUTPUT is a logic one, keeper 23 is OFF. The keeper circuit of Claim 10 has a keeper input coupled to the complementary output of the static logic circuit and a keeper output coupled to the dynamic node. Since the output of inverter 23 of Bernstein is the output, the keeper of Bernstein does not have a keeper input coupled to the complementary output and a keeper output coupled to the dynamic node. The keeper of Bernstein is coupled between the OUTPUT and the dynamic node and note between the complementary output of the static logic circuitry that provides the latching function and the dynamic node as recited in Claim 10 of the present invention.

Therefore, the Applicant respectfully asserts that the rejection of Claim 10 under *35 U.S.C. § 102(b)*, as being anticipated by *Bernstein* is traversed by the amendments to Claim 10 and the above arguments.

Claim 11 is dependent from Claim 10 and contains all the limitations of Claim 10. Claim 11 adds the limitation that keeper circuit is a PFET having a gate terminal coupled to the complementary output (of the static logic circuit), a source terminal coupled to the power supply terminal, and a drain terminal coupled to the dynamic node. While Bernstein does disclose a PFET keeper device, it has its gate terminal coupled to an OUTPUT of an inverter 26 and not the complementary output of the static logic circuitry with the latching function of Claim 10. The Applicant has shown that Bernstein does not anticipate Claim 10. Therefore, the Applicant respectfully asserts that the rejection of Claim 11 under *35 U.S.C. § 102(b)*, as being anticipated by *Bernstein* is traversed by the above arguments and for the same reasons as Claim 10.

II REJECTION UNDER 35 U.S.C. § 103

The Examiner rejected Claims 1-9 under *35 U.S.C. § 103(a)*, as being unpatentable over *Bernstein* in view of U.S. Patent No. 6,496,038 B1 to *Sprague et al.* (hereafter "*Sprague*").

The Examiner states that *Bernstein* teaches all the features of the claimed invention; however, the Examiner does not specifically address Claim 1 which has different claim language from Claim 10 which the Applicant has shown is not anticipated by *Bernstein*. However, relative to Claims 1-9, the Examiner states that Bernstein teaches all the features of the claimed invention with the exception of the claimed static logic circuitry. The Examiner then states that *Sprague* teaches "the static logic circuitry to provide a static signal from a dynamic node and acts as an interface between dynamic and static environments without pointing out what he considers the static logic circuitry of *Sprague*." In one case, the Examiner states that Bernstein anticipates the static logic circuitry and then the Examiner states that Bernstein does not teach this limitation. Understanding what the Examiner considers the static logic circuitry is important because in Claim 1 the keeper circuitry is coupled to the static logic circuitry in a particular way. The Applicant asserts that the Examiner has failed to make a *prima facie* case of obviousness for failing to specifically point out what he considers the static logic

circuitry of *Sprague*. If the blocks labeled "STATIC 230A-230D" are considered the static logic circuitry of *Sprague*, then the Applicant asserts that there is no keeper circuitry that is coupled in any manner to this circuitry. If circuitry 220 is considered the static logic circuitry, then the output is node 267 and the complementary output is the output of inverter 265. As one can see, there is no keeper circuit having a keeper input coupled to the complementary output and a keeper output coupled to the dynamic node 237. The Applicant asserts that the Examiner has failed to specifically address the limitations of Claim 1. Likewise, the Applicant asserts that the Examiner has failed to point out what he considers the static logic circuitry of *Sprague* that the Examiner believes teaches the static logic circuitry in the invention of Claim 1. Further, the Applicant has shown that the circuits of *Sprague,* that could possibly generate the output and the complementary output of the static logic circuitry of Claim 1, are not coupled to a keeper circuit that is coupled to the dynamic node as recited in Claim 1. Therefore, the Applicant respectfully asserts that the rejection of Claim 1 under *35 U.S.C. § 103(a)*, as being unpatentable over *Bernstein* in view of *Sprague* is traversed by the above arguments.

Claims 2-3 are dependent from Claim 1 and contain all the limitations of Claim 1. The Applicant asserts that the Examiner has failed to make a *prima facie* case of obviousness for failing to specifically address Claims 2-3. Therefore, the Applicant asserts that the rejections of Claims 2-3 under *35 U.S.C. § 103(a)*, as being unpatentable over *Bernstein* in view of *Sprague* are traversed for the above arguments and for the same reasons as Claim 1.

Claim 4 is an independent claim directed to a logic device implementing the dynamic logic circuitry of Claim 1. The Applicant asserts that the Examiner has failed to make a *prima facie* case of obviousness by failing to specifically address the invention of Claim 4. Therefore, the Applicant asserts that the rejection of Claim 4 under *35 U.S.C. § 103(a)*, as being unpatentable over *Bernstein* in view of *Sprague* is traversed for the above arguments and for the same reasons as Claim 1.

Claims 5-6 are dependent from Claim 4 and contain all the limitations of Claim 4. The Applicant has shown that the Examiner has failed to make a *prima facie* case of obviousness by failing to specifically address the invention of Claim 4. Likewise, the Examiner has failed to specifically address Claims 5-6. Therefore, the Applicant asserts that the rejections of Claims 5-6 under *35 U.S.C. § 103(a)*, as being unpatentable over *Bernstein* in view of *Sprague* are traversed for the above arguments and for the same reasons as Claim 1.

Claim 7 is an independent claim directed to a data processing system having the logic device of Claim 4 implementing the dynamic logic circuitry of Claim 1. The Applicant asserts that the Examiner has failed to make a *prima facie* case of obviousness by failing to specifically address the invention of Claim 7. The Examiner has made a broad statement that the way the apparatus is intended to be employed does not differentiate the claimed apparatus from the prior art. The Applicant has shown that *Bernstein* and *Sprague*, singly and in combination, do not teach or suggest the invention of Claim 1. Therefore, these references cannot read on a data processing system of Claim 7 that has the logic device of Claim 4 incorporating the dynamic logic circuitry of Claim 1. Therefore, the Applicant asserts that the rejection of Claim 7 under *35 U.S.C. § 103(a)*, as being unpatentable over *Bernstein* in view of *Sprague* is traversed for the above arguments and for the same reasons as Claims 1 and 4.

Claims 8-9 are dependent from Claim 7 and contain all the limitations of Claim 7. The Applicant has shown that the Examiner has failed to make a *prima facie* case of obviousness by failing to specifically address the limitations of the invention of Claim 7. Likewise, the Examiner has failed to specifically address the limitations of Claims 8-9. Therefore, the Applicant asserts that the rejections of Claims 8-9 under *35 U.S.C. § 103(a)*, as being unpatentable over *Bernstein* in view of *Sprague* are traversed for the above arguments and for the same reasons as Claims 1, 4 and 7.

III. CONCLUSION

The Applicant has amended the claim language of Claims 1, 4, 7, and 10 after discussion with the Examiner to clarify the differences between the present inventions and the prior art.

The Applicants, therefore, respectfully assert that amended Claims 1, 4, 7, and 10, and Claims 2-3, 5-6, 8-9, and 11 are now in condition for allowance and request an early allowance of these claims.

Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

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